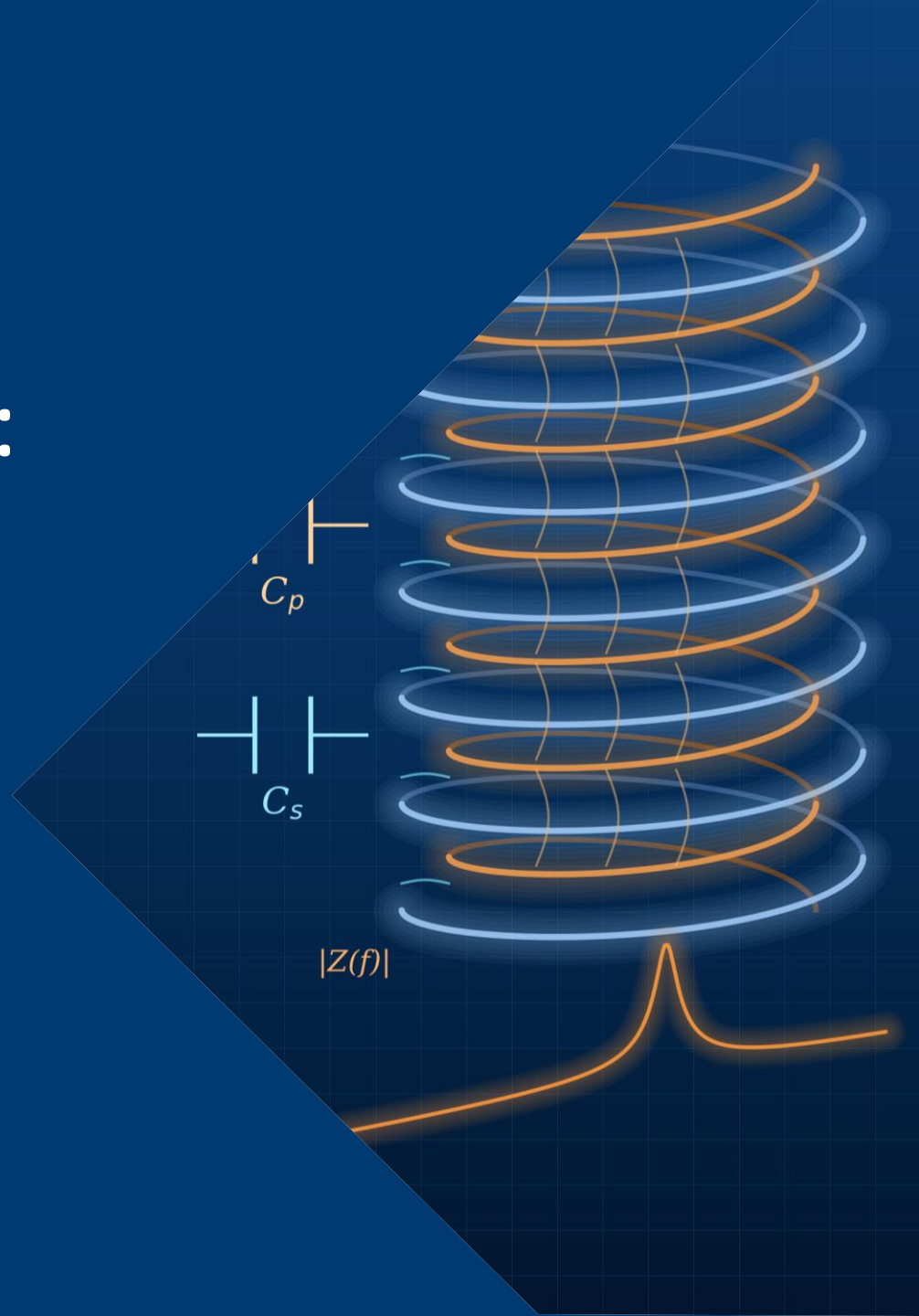
ECT
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Beyond the Ideal Transformer: When Picofarads Matter in MHz Power Conversion

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Muhammad Ehab | Lecturer, Power Electronics



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Introduction – Presenter

Muhammad Ehab



- Lecturer and tutor in power electronics and power systems at EIT
- PhD candidate, The University of Western Australia
- M.S. Electrical Engineering, Soongsil University, Seoul (2022): high-frequency transformer modelling and inductive–capacitive power transfer
- B.S. (Hons.) Electrical Engineering, The University of Lahore (2019)
- Research: MHz power conversion, magnetics and parasitics, wireless power transfer, grid-connected inverters, solid-state transformers

Agenda

	Section	Approx.
1	Why picofarads matter at MHz	7 min
2	What the literature offers	8 min
3	A physics-based lumped transformer model	7 min
4	Validation from 1 to 30 MHz	6 min
5	13.56 MHz hardware: from fighting to using parasitics	9 min
6	Design guidance	8 min



Part 1 of 6

Why picofarads matter at MHz

Frequency scaling, hidden capacitances and what they do to a converter

Why push isolated converters into the MHz range?

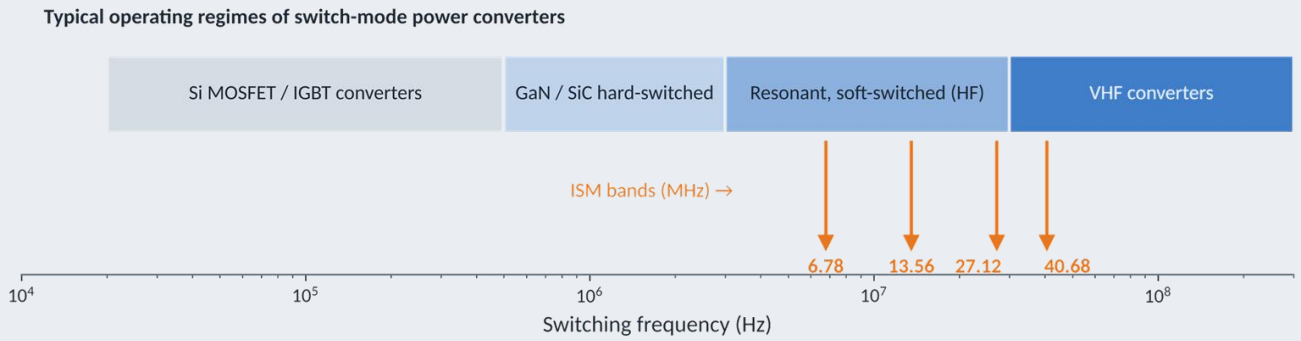


Fig. 1. Operating regimes of switch-mode converters and the ISM bands [1], [2].

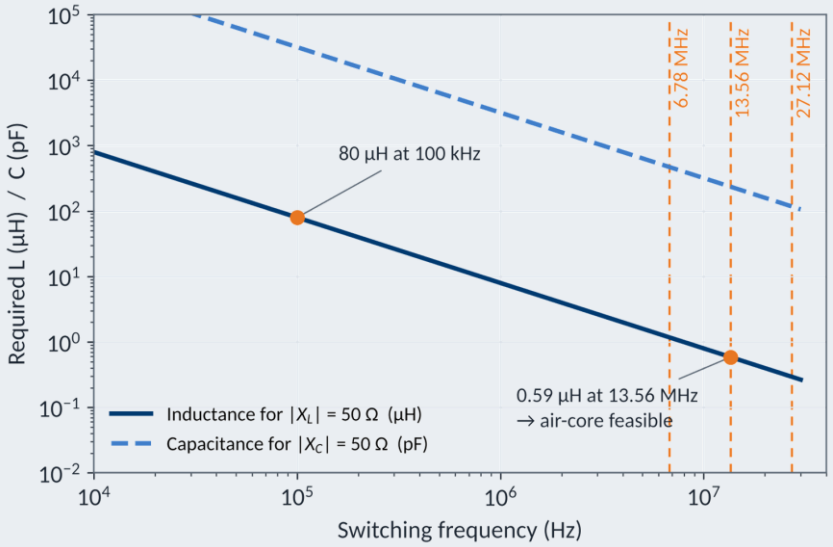


Fig. 2. Inductance and capacitance needed for a 50 Ω reactance.

- **Passive size scales as 1/f**: 50 Ω of reactance needs 80 µH at 100 kHz but only 0.6 µH at 13.56 MHz, so air-core magnetics become practical [1]
- GaN makes soft-switched 6.78–13.56 MHz converters real: 200–400 W dc–dc [3], 1.3 kW WPT inverter [4], 15 W isolated gate-driver supply [5]
- But every picofarad and nanohenry now matters

Anatomy of an isolated resonant converter

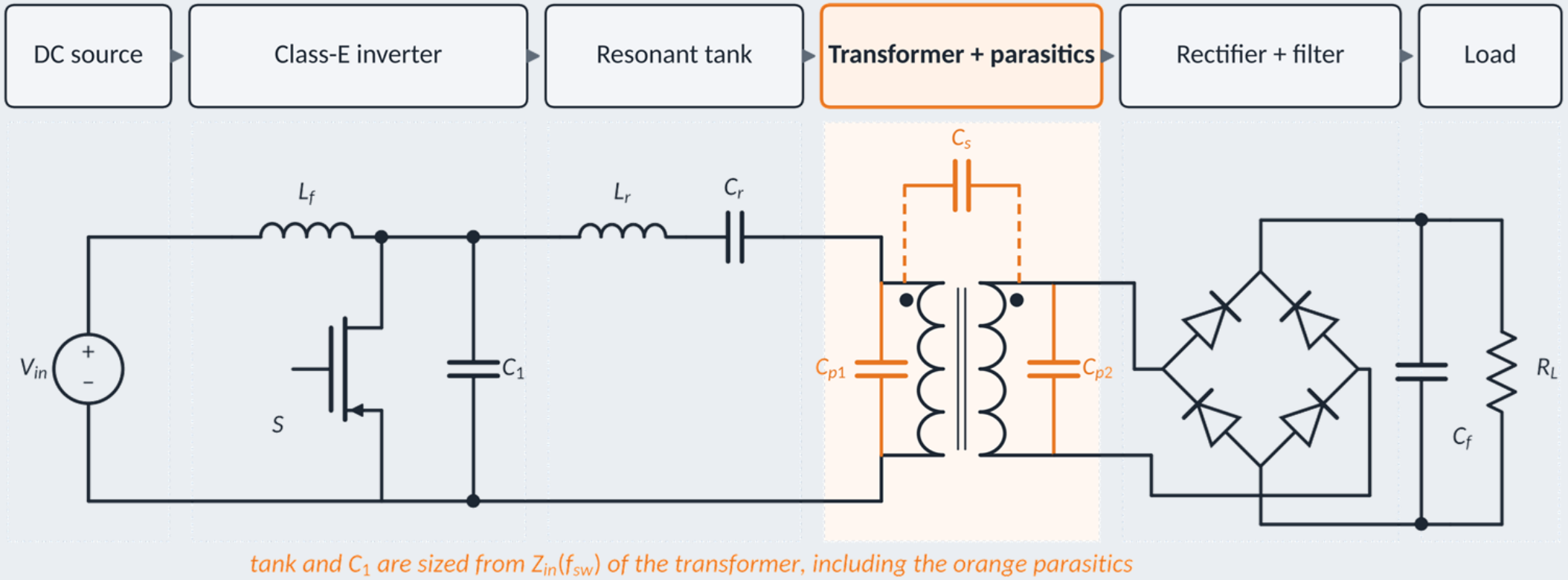
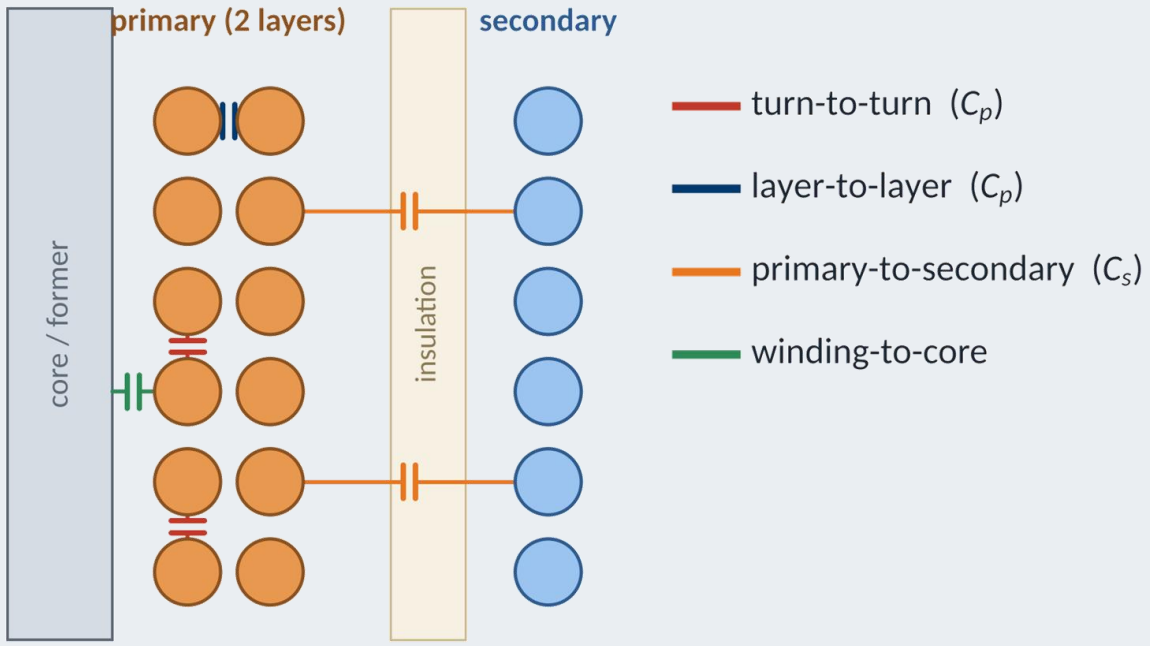


Fig. 3. Isolated Class-E converter: the tank and C_1 are designed from the transformer's input impedance [6], [7].

› Any error in $Z_{in}(f_{sw})$, e.g. unmodelled orange capacitances goes straight into the switch waveform

Where the parasitic capacitances hide



energy ½CV² is stored wherever conductors at different potentials face each other

Fig. 4. Capacitances inside a two-winding transformer (cross-section) [8], [9].

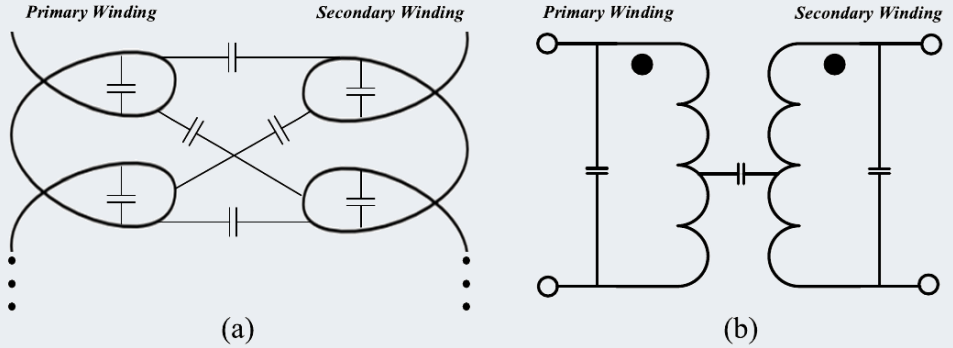


Fig. 5. Distributed capacitance (a) lumped into three capacitors (b) [10].

- **Intrawinding C_p**: turn-to-turn and layer-to-layer; sets the winding self-resonance [11]
- **Interwinding C_s**: across the isolation barrier; carries common-mode current
- Lumped values preserve the stored energy ½CV² [9]

Why a picofarad matters at MHz

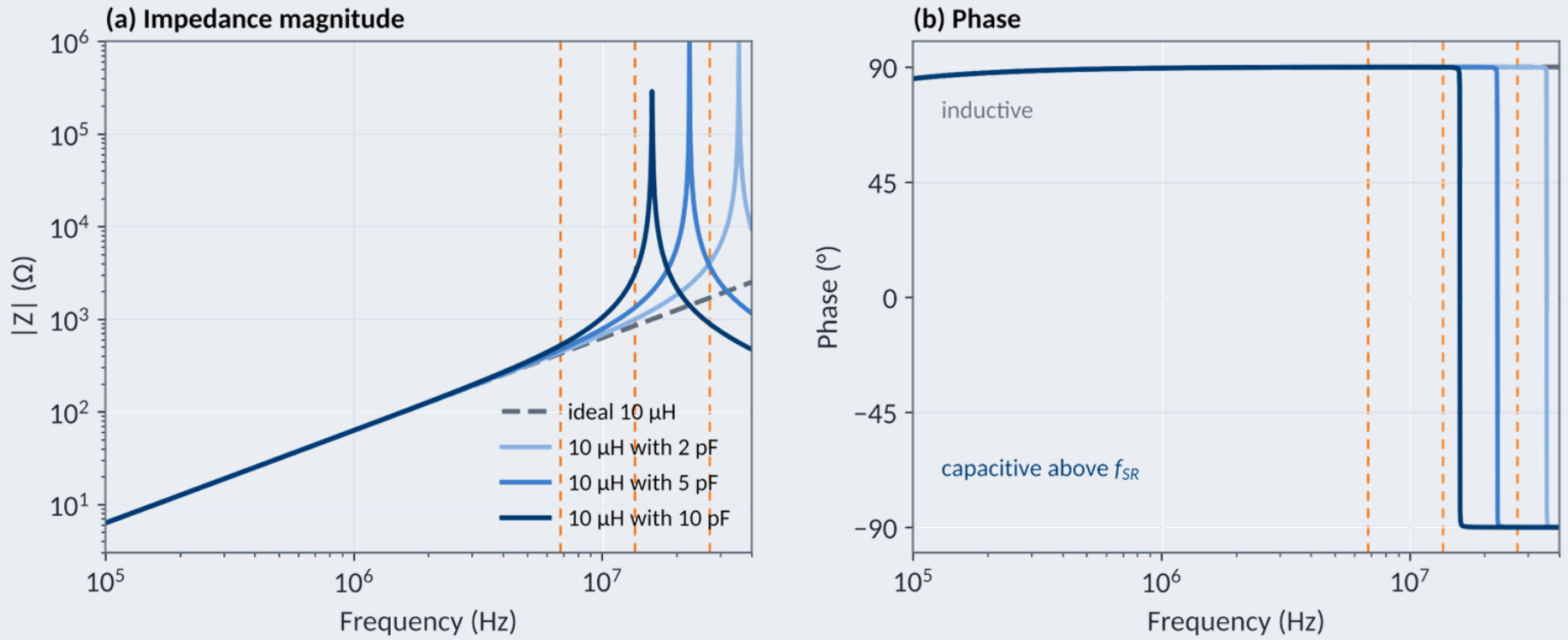


Fig. 6. A 10 µH winding with 2–10 pF of self-capacitance: self-resonance falls into the ISM bands and the winding turns capacitive above it [11].

318 kΩ
5 pF at 100 kHz

2.3 kΩ
the same 5 pF at 13.56 MHz

22.5 MHz
10 µH + 5 pF self-resonance

What the parasitics do to a converter

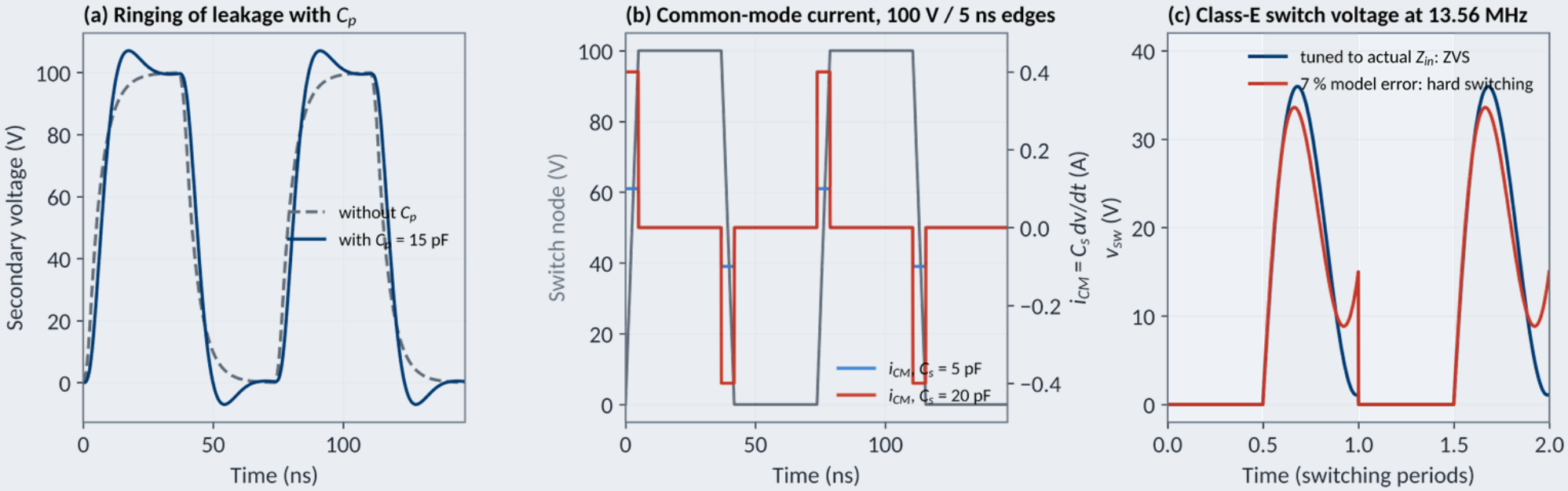


Fig. 7. Simulated consequences: (a) ringing, (b) common-mode current through C_s, (c) loss of ZVS in a Class-E stage [12].

Ringing and overshoot

Leakage resonates with C_p: extra voltage stress on rectifier diodes and radiated noise [9]

Common-mode EMI

$i_{CM} = C_s \cdot dv/dt$: 20 pF on a 20 V/ns edge already gives 0.4 A spikes; interleaving makes it worse [13]

Lost soft switching

A 7 % error in the tank's view of Z_{in} gives hard turn-on at 15 V and $\frac{1}{2}C_1V^2f$ loss every cycle

Part 2 of 6

What the literature offers

Thirty years of high-frequency transformer models, and where they stop

Thirty years of high-frequency transformer modelling

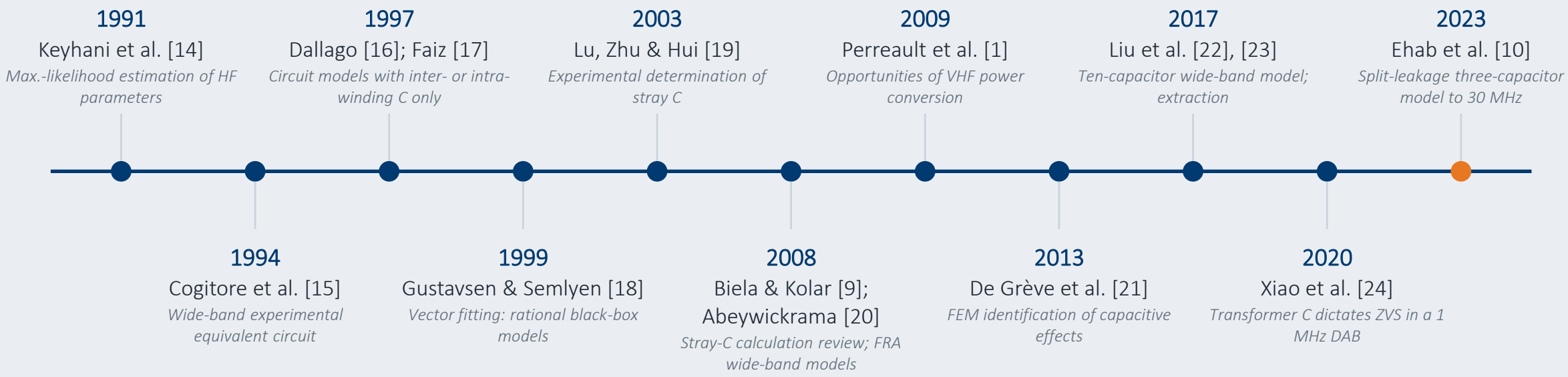


Fig. 8. Selected milestones in high-frequency transformer modelling.

Lumped equivalent circuits in the literature

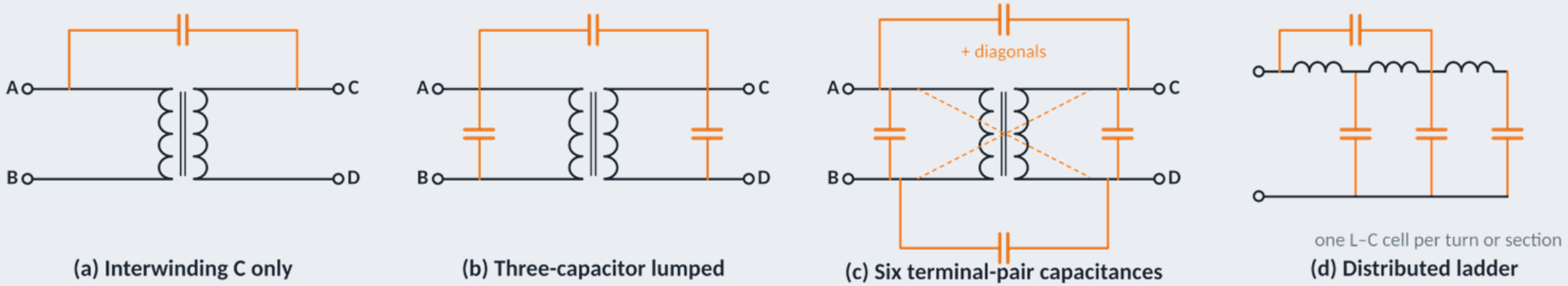


Fig. 9. Typical capacitive extensions of the transformer T-model [9], [15], [17], [20].

Table I. How far the lumped models have been validated, as reported in the literature [10].

Model	Capacitive elements	Validated to	Main limitation
Interwinding or intrawinding only [16], [17]	1–2	kHz range	Misses one family of capacitance
Three-capacitor [14], [15]	3	60 Hz – kHz units	C_p placed across the terminals
Six / ten-capacitor, FEM [21], [22]	6–10	≤ 300 kHz	Parameters hard to measure
Multi-section ladder [20]	> 10	≤ 1 MHz	No closed-form Z_{in} for design

Three ways to obtain the capacitances

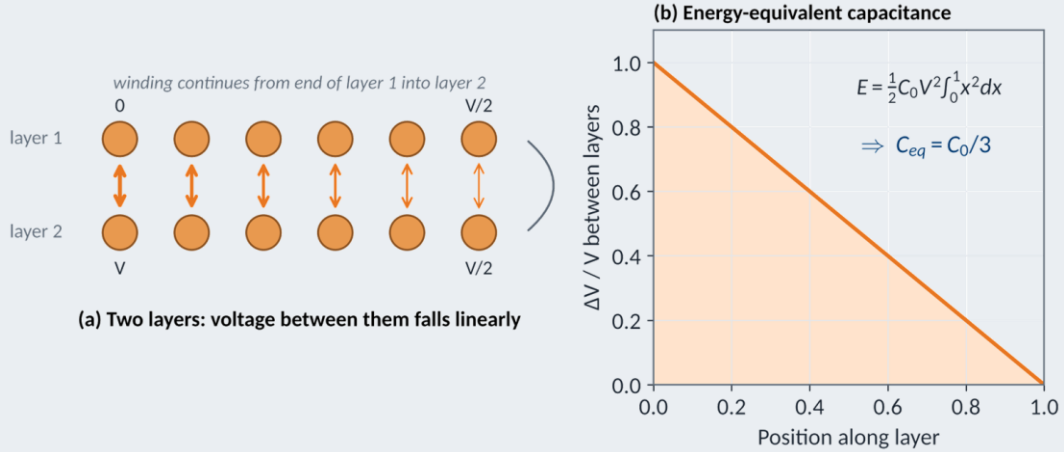


Fig. 10. Energy method: two layers of one winding store $C_0V^2/6$, so $C_{eq} = C_0/3$ [9].

- **Analytical** formulae give insight before a prototype exists [8], [9]
- **FEM** handles complex geometry but is slow [21]; static-field formulae hold only to a few hundred kHz [25]
- **Measurement** captures the real build, tolerances and fixtures [19], [23]

Table II. Comparison of capacitance-extraction approaches.

Approach	Strength	Limitation
Analytical (geometry, energy)	Fast; links C to pitch, layers, insulation	Idealised geometry; misses fringing
Numerical (FEM)	Any geometry; many capacitances	Slow; many parameters to identify
Measurement-based lumped	Real build; physically meaningful	Needs prototype and impedance analyser
Black-box fitting [18]	Very wide bandwidth	No physical insight for design

More capacitors is not the same as more bandwidth

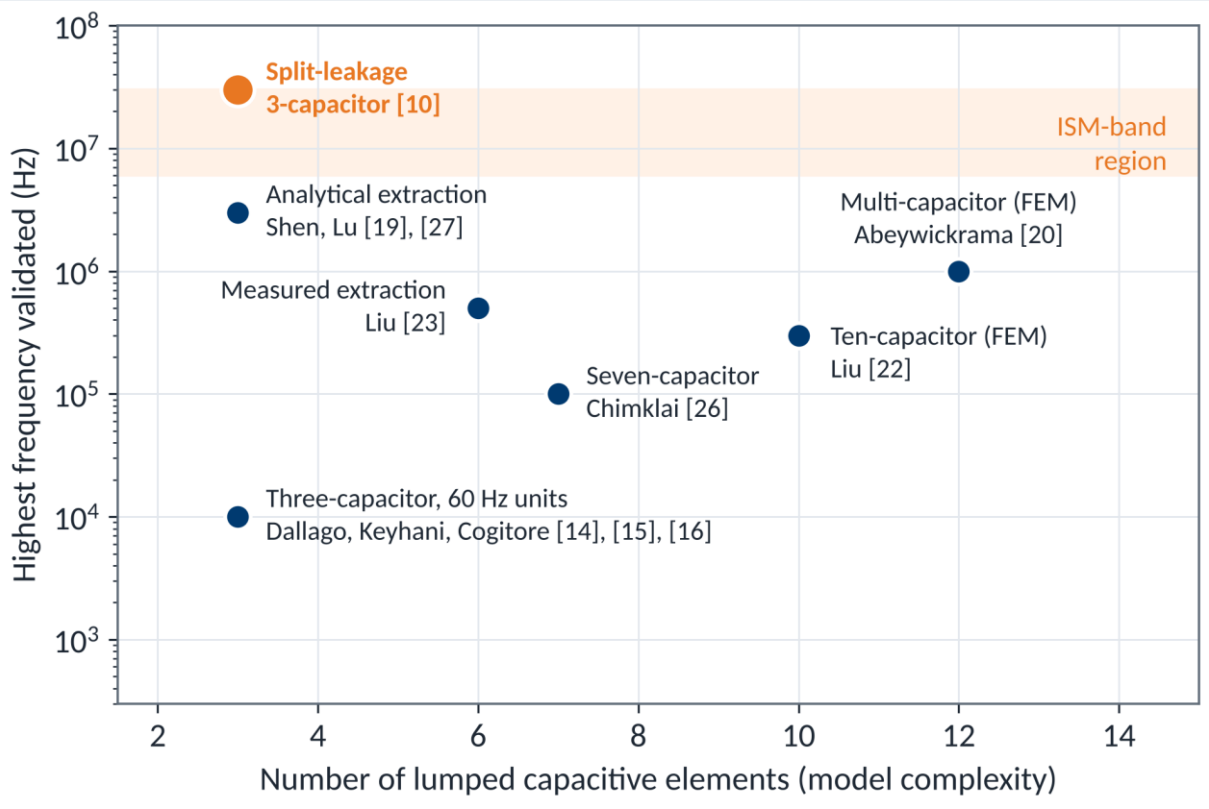


Fig. 11. Model complexity against highest validated frequency [10].

Gaps in the literature

- Nearly all models validated **below 1 MHz**
- Little guidance on **how to measure** parameters
- No closed-form Z_{in} for converter design

What a design model needs

- Lumped and physically meaningful
- Parameters from a few simple measurements
- Closed-form impedance and gain
- Valid to **30 MHz** (three ISM bands)

Recent converters shaped by transformer capacitance

Table III. Selected recent works and the role of transformer or coil capacitance.

Work	Converter	Role of capacitance / lesson
Liang et al. [3]	13.56 MHz, 200–400 W dc–dc	Air-core PCB inductors keep values stable for tuning
Choi et al. [4]	13.56 MHz, 1.3 kW Class Φ_2	GaN inverter for WPT; tank tuned to coil impedance
Spro et al. [5]	6.78 MHz, 15 W isolated	> 40 kV insulation with coupling C < 10 pF
Arteaga et al. [28]	13.56 MHz, 1-to-4 outputs	Coil overlap sets coupling between receivers
Xiao et al. [24]	1 MHz GaN DAB	Split series L across both sides restores ZVS
Wang et al. [29]	200 W LLC, 400→12 V	Measured C in dead-time design: 94.2 %
Saket et al. [13]	Flyback / forward	Paired layers cancel CM current (≈20 dB)

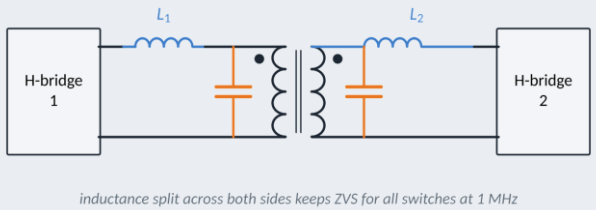


Fig. 12. DAB with series inductance split across the transformer [24].

Common thread

- Tune to the **measured** impedance at f_{sw}
- Minimise C_s for isolation and EMI, or absorb it into the resonant network

Part 3 of 6

A physics-based lumped model

Split leakage, three capacitors, five measurements

Proposed model: split leakage plus three capacitors

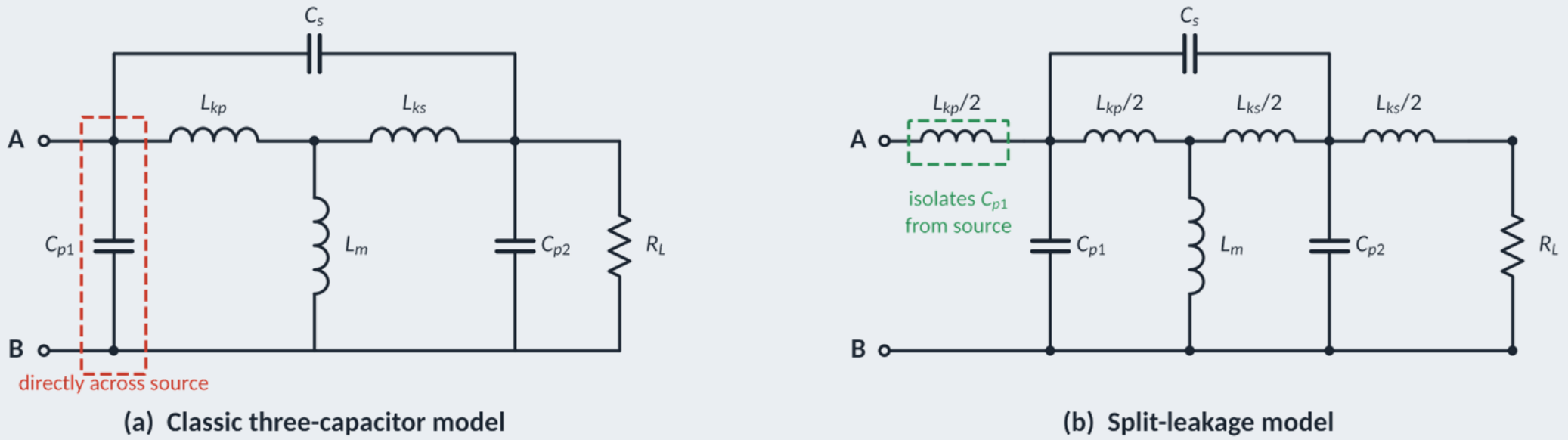


Fig. 13. (a) Classic three-capacitor model; (b) proposed split-leakage model [10].

- In (a), C_{p1} sits across a stiff voltage source, so it cannot shape the impedance as a real winding does
- Each turn is a small L–C cell, so splitting the leakage places C_p **between** the halves; leakage dominates at MHz

One model, three energy-transfer paths

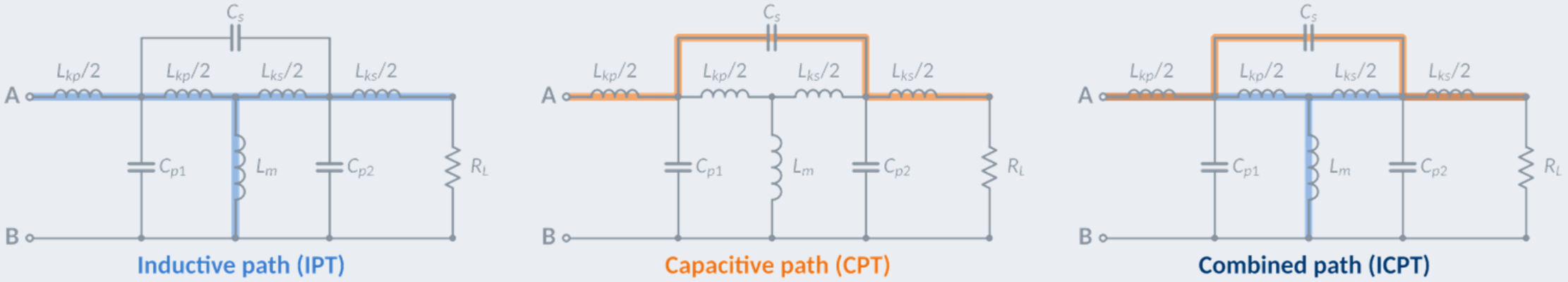


Fig. 14. Inductive (blue), capacitive (orange) and combined energy paths in the same model [6], [10].

IPT

Power through L_m; capacitances are parasitic, the conventional transformer

CPT

Power through C_s; inductances are parasitic, capacitive power transfer

ICPT

L_m and C_s both carry power, inductive–capacitive transfer [30]

Five measurements give all nine parameters



Fig. 15. Open- and short-circuit tests give L_{oc} and L_{sc} [6].

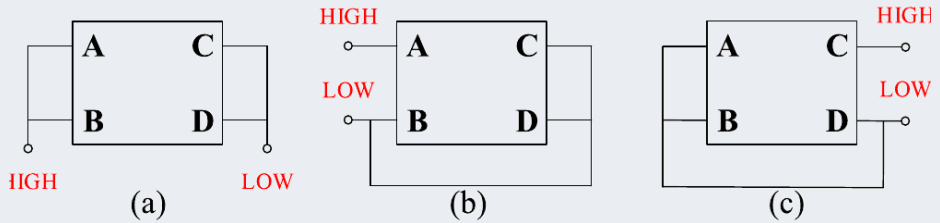


Fig. 16. Shorting tests for C_s, C_{p1}, C_{p2} [10].

$$k = \sqrt{1 - \frac{L_{sc}}{L_{oc}}} \qquad L_m = k\,L_{oc} \qquad L_{kp} = (1-k)\,L_{oc}$$

$$C_{p1} = C_{m1} - C_s \qquad C_{p2} = C_{m2} - C_s$$

- One sweep per test with an impedance analyser (HP 4194A, dc–40 MHz fixture)
- Read values well below the first resonance
- Short both windings → C_s directly
- Short the other side → $C_p + C_s$, then subtract
- No FEM and no curve fitting [19]

Closed-form input impedance and voltage gain

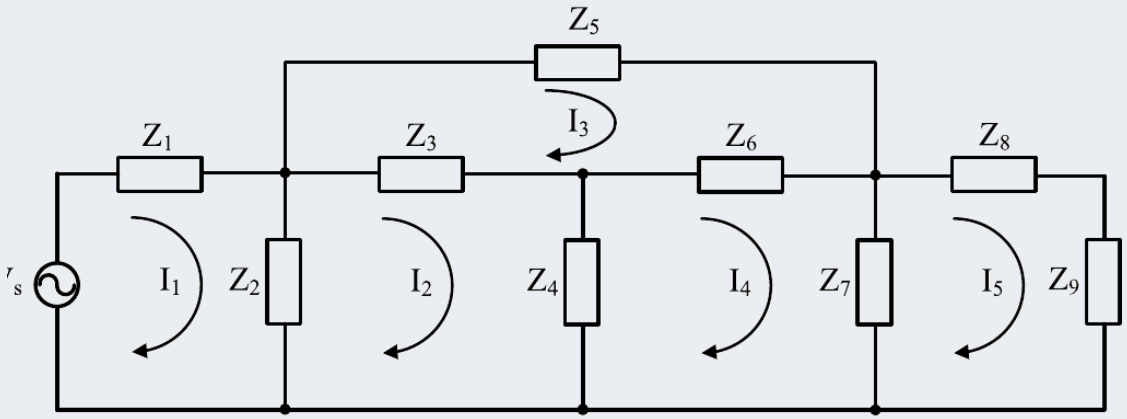


Fig. 17. Mesh equivalent of the model (symmetric case) [10].

$$Z_{1,3,6,8} = s\frac{L_k}{2} + \frac{R_w}{2}, \quad Z_{2,7} = \frac{1}{sC_p}, \quad Z_4 = sL_m, \quad Z_5 = \frac{1}{sC_s}, \quad Z_9 = R$$

- Five mesh equations, solved symbolically: all coefficients are explicit functions of the nine parameters

$$Z_{in}(s) = \frac{a_6 s^6 + a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0}$$

$$G_v(s) = \frac{a_3 s^3 + a_2 s^2 + a_1 s}{b_6 s^6 + b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0}$$

- $Z_{in}(j2\pi f_{sw})$ gives R and X directly for tank and C_1 design
- Poles and zeros mark the series and parallel resonances
- Fast enough for tolerance sweeps; general and symmetric cases in [10]

Part 4 of 6

Validation from 1 to 30 MHz

Five transformers, two geometries,
two loads, two couplings

Five test transformers

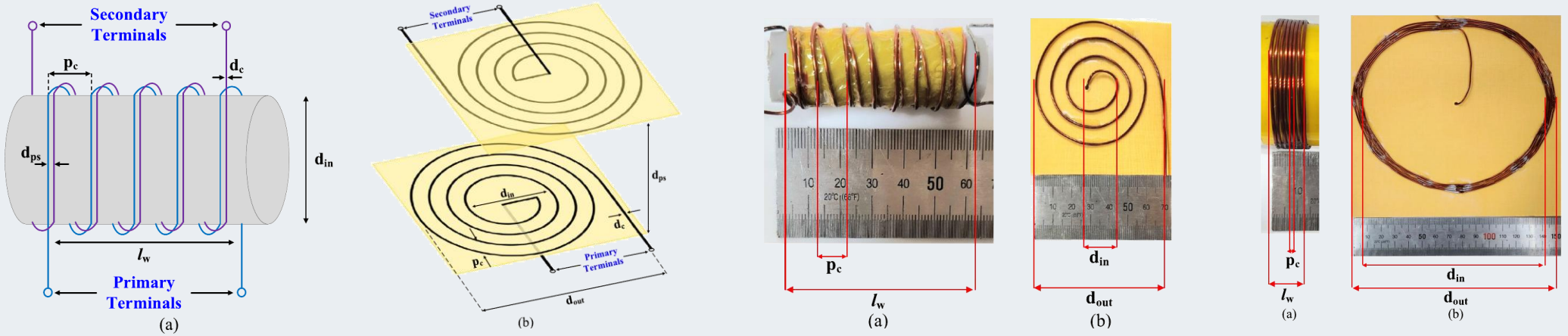
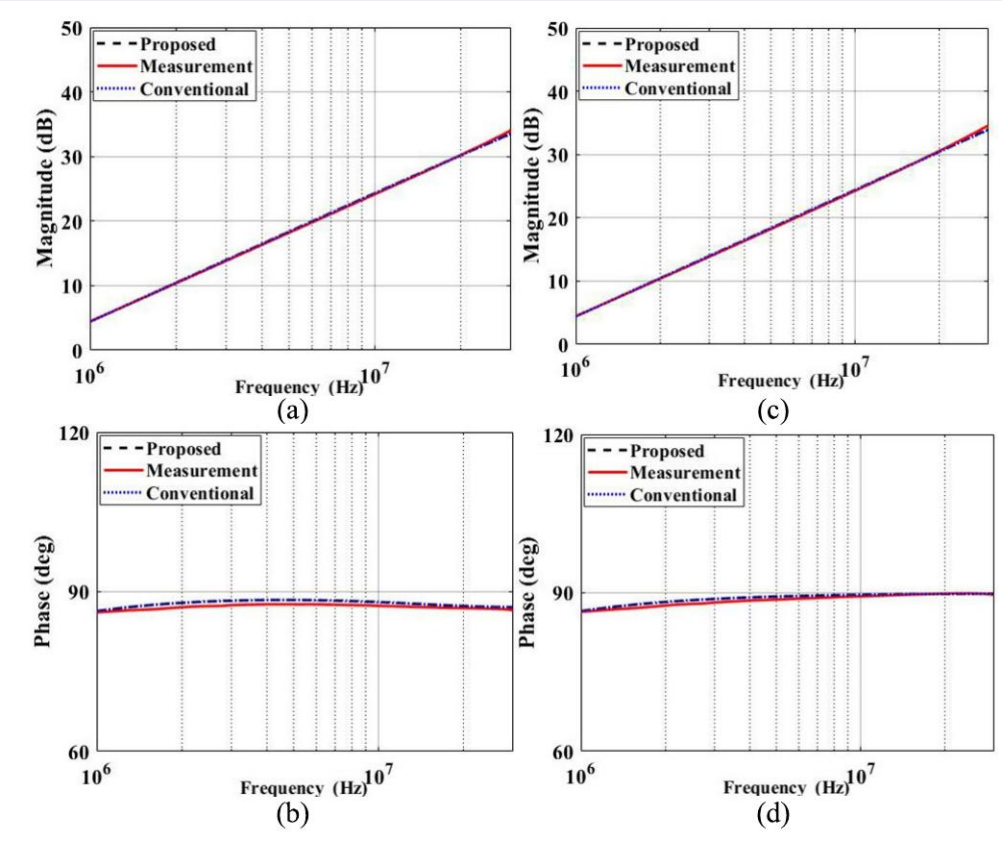


Fig. 18. Schematics (left) and fabricated low- and high-parasitic transformers (right) [10]. Fabricated transformers (left to right): CS1, CS2, CS3, CS4 and CS5.

Table IV. Geometry and measured parameters [10].

Case	Geometry	Pitch	L_k	L_m	C_p	C_s
CS1	Solenoid, 7 turns	10 mm	0.19 µH	0.4 µH	2 pF	1 pF
CS2	Spiral, 4 turns	10 mm	0.18 µH	0.08 µH	1 pF	1 pF
CS3	Solenoid, 7 turns	2 mm	0.82 µH	4.5 µH	4.2 pF	7 pF
CS4, k = 80 %	Spiral, 5 turns	0.6 mm	3.76 µH	7.2 µH	7.5 pF	4 pF
CS5, k = 60 %	Spiral, 3 : 9 turns	0.5 mm	1 / 0.87 µH	1.4 µH	5 / 55 pF	5 pF

Low versus high parasitics



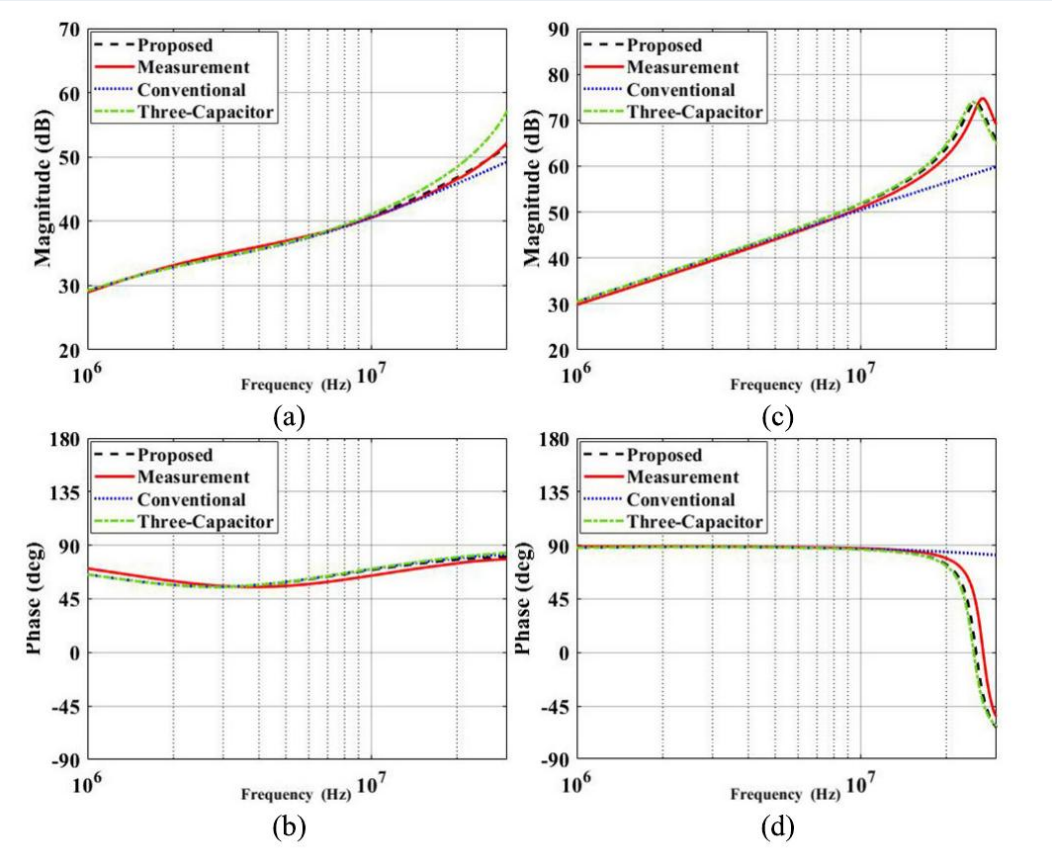
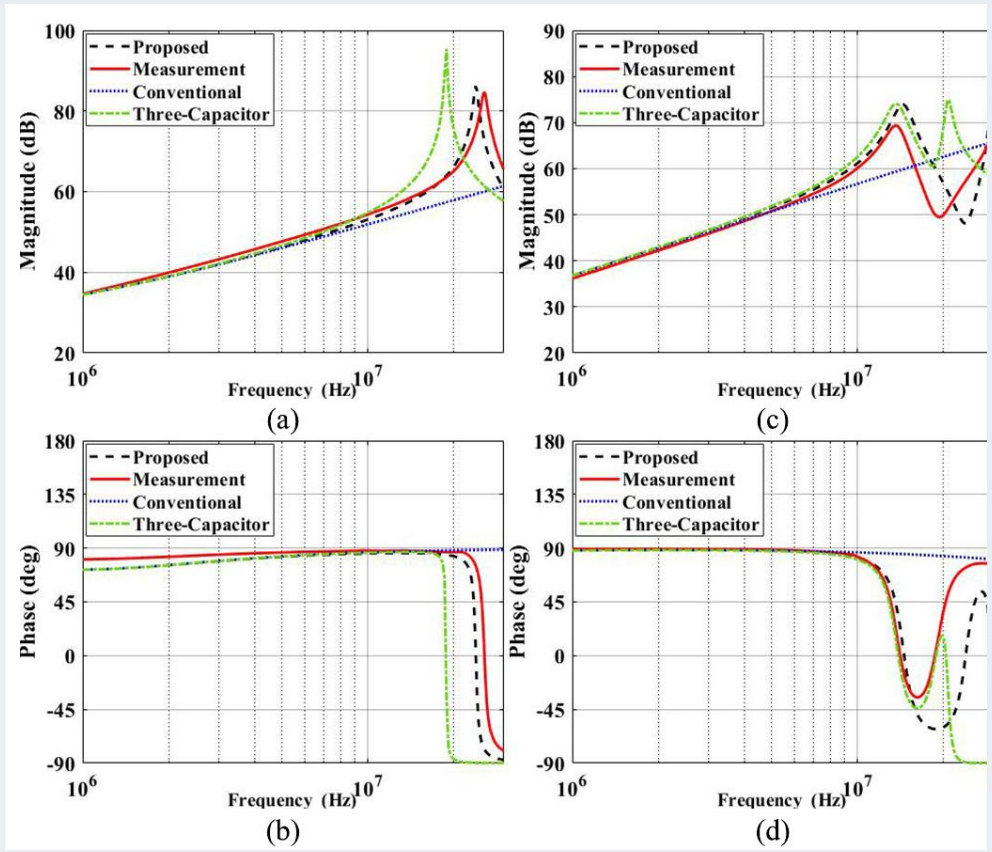


Fig. 19. Measured and modelled Z_{in}: CS1 loose solenoid (left) and CS3 compact solenoid (right); (a, b) 50 Ω, (c, d) 5 kΩ [10].

› Loose winding: every model fits. Compact winding: resonance at **26.5 MHz** and phase falling below zero. The inductive model cannot follow

Coupling moves the resonances (CS4 spiral)



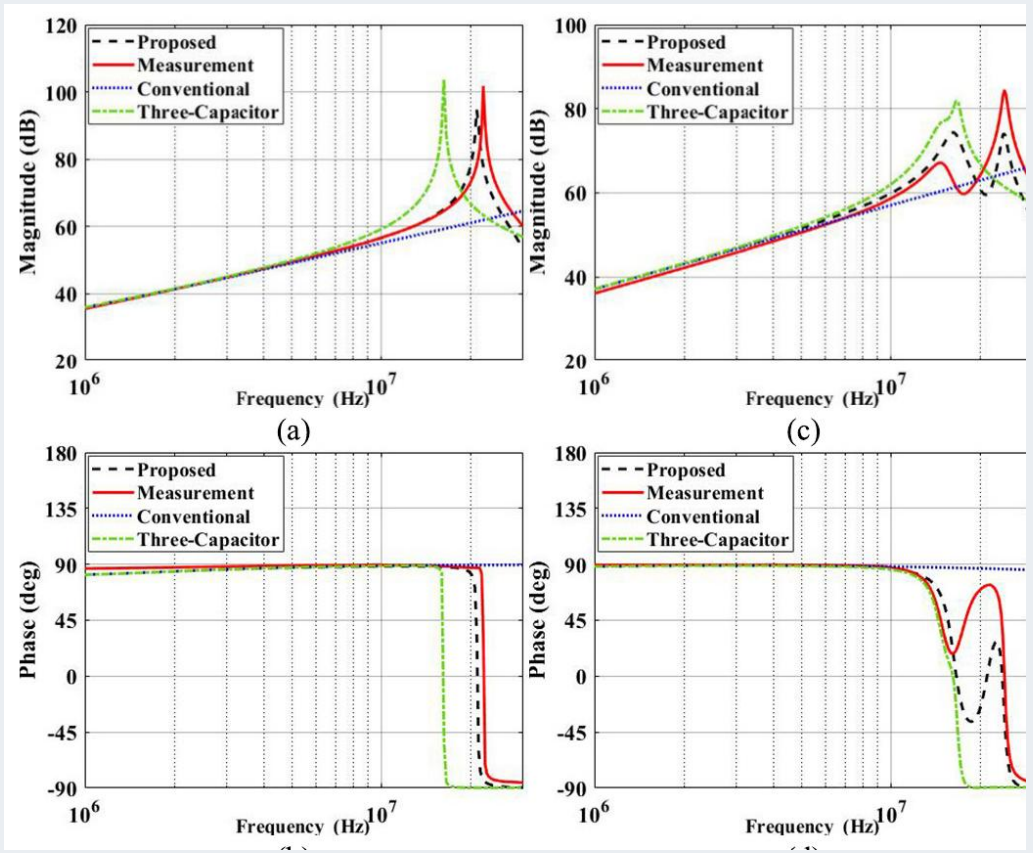


Fig. 20. CS4 at k = 80 % (left, 0.3 cm gap) and k = 40 % (right, 2 cm gap) [10].

› Peaks move 25.6 → 22 MHz (heavy) and 13.4 → 15 MHz, > 30 → 24 MHz (light); the proposed model tracks them, the three-capacitor model misplaces them

Non-unity turns ratio and robustness

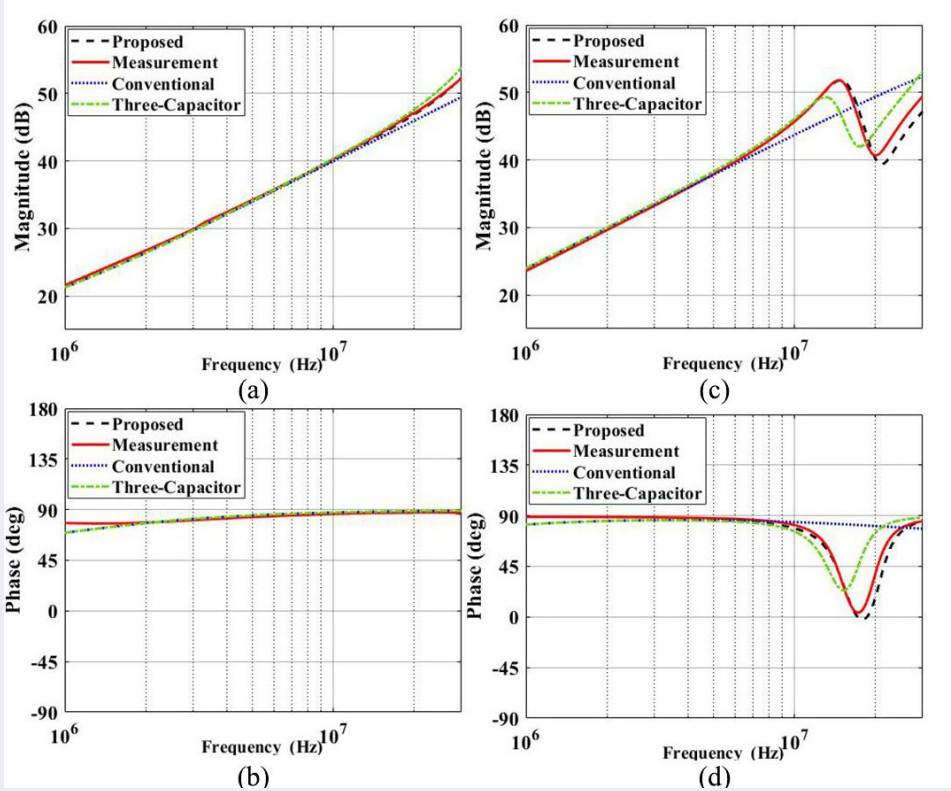


Fig. 21. CS5 (1 : 3) at k = 60 % [10].

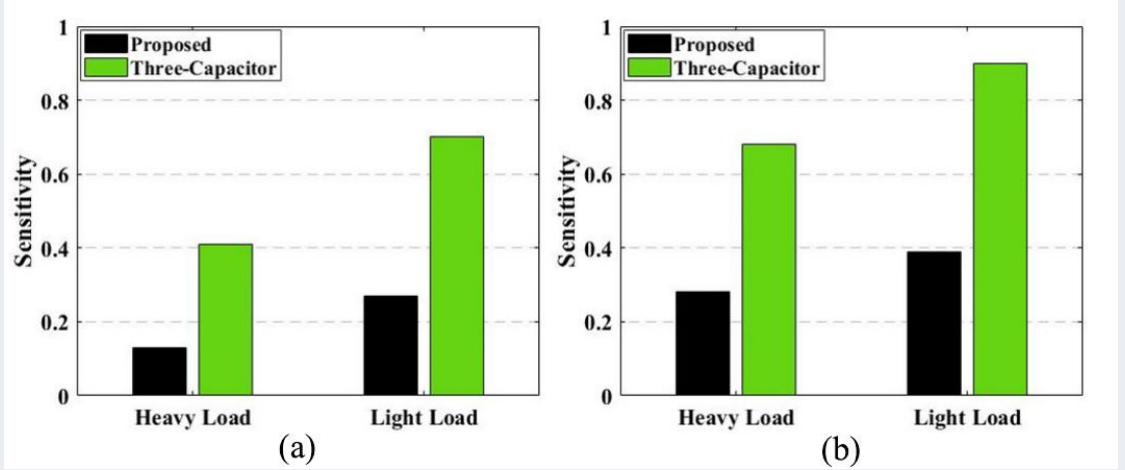


Fig. 22. Sensitivity of Z_{in} to ±20 % winding spacing: (a) magnitude, (b) phase [10].

- Referred to the primary, the 1 : 3 transformer fits the same model
- Proposed model is 2–3× **less sensitive** to spacing error than the three-capacitor model
- CS5's Z_{in} at 13.56 MHz feeds the converter design next

Part 5 of 6

13.56 MHz hardware

Same transformer, three models —
then using the parasitics on purpose

Test bench: isolated Class-E inverter at 13.56 MHz

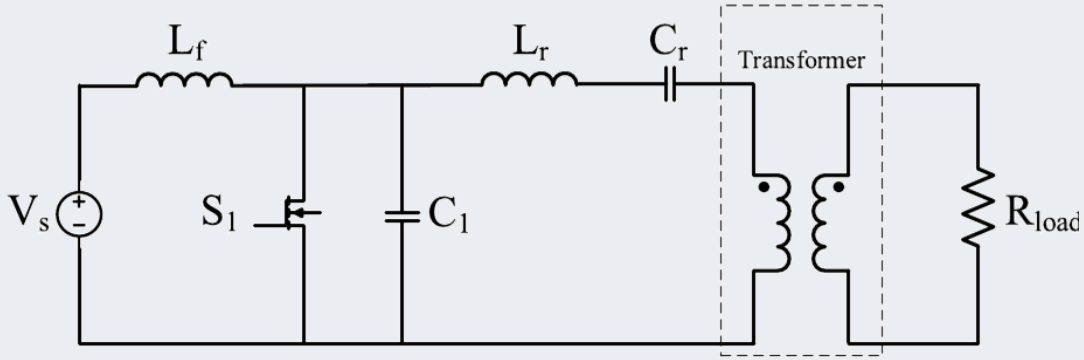


Fig. 23. Isolated Class-E inverter with the CS5 transformer [10].

- EPC9083 GaN board, 10 V input, 10 µH choke, 50 Ω load
- L_r, C_r, C_1 designed for ZVS from each model's Z_{in}
- Only the **transformer model** differs between the three builds

Table V. Class-E parameters from each transformer model [10].

Parameter	Conventional	Three-cap.	Proposed
Model Z_{in}	135 Ω ∠88°	152 Ω ∠88°	145 Ω ∠87°
Shunt C_1	450 pF	410 pF	280 pF
Resonant L_r	1.57 µH	1.79 µH	1.7 µH
Resonant C_r	100 pF	78 pF	85 pF

135–152 Ω but C_1 from 280 to 450 pF
similar impedances, very different tank designs

Switch waveforms: only the proposed model achieves ZVS

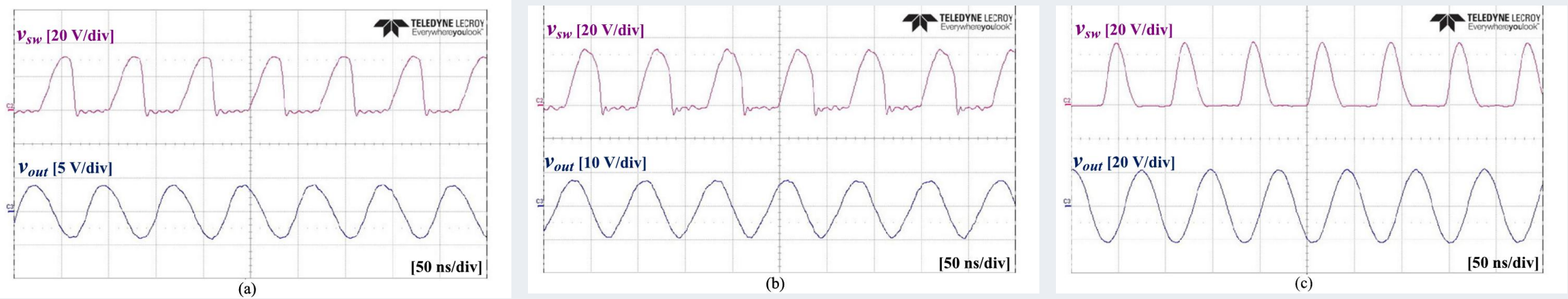


Fig. 24. Measured v_{sw} (top, 20 V/div) and v_{out} (bottom), 50 ns/div: design from (a) conventional, (b) three-capacitor, (c) proposed model [10].

(a) Conventional

Hard turn-on, far from the real resonance; v_{out} at 5 V/div

(b) Three-capacitor

Better, but still hard-switched and off-resonance

(c) Proposed

v_{sw} reaches zero before turn-on: **ZVS**; v_{out} at 20 V/div

Efficiency and thermal stress

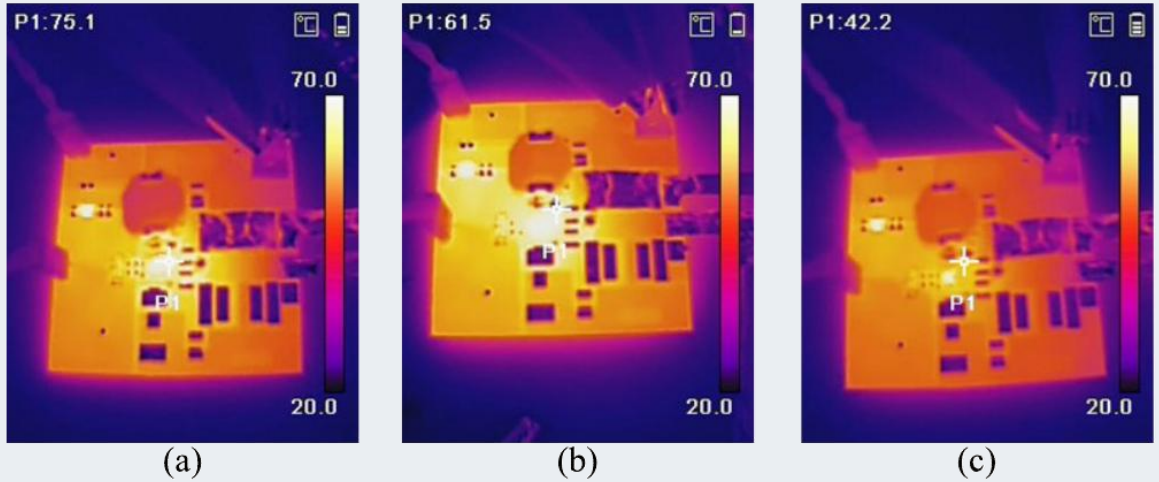


Fig. 25. Steady-state thermal images: (a) conventional, (b) three-capacitor, (c) proposed design [10].

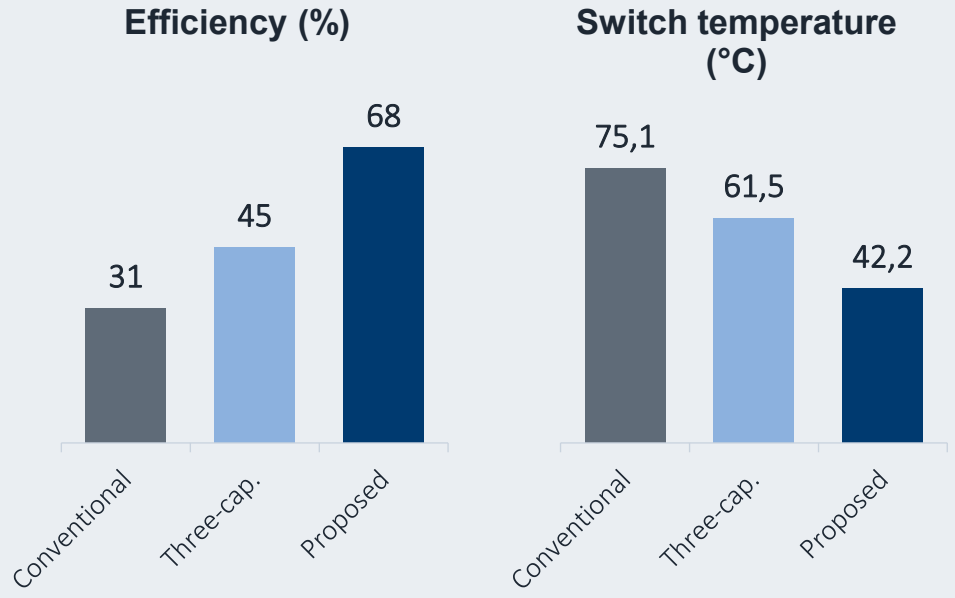


Fig. 26. Measured efficiency and switch temperature [10].

31 % → 68 %
efficiency

75.1 → 42.2 °C
switch temperature

- Lower switch stress → more power from the same hardware
- The only change was the **transformer model**

Using the parasitics: an inductive–capacitive transformer

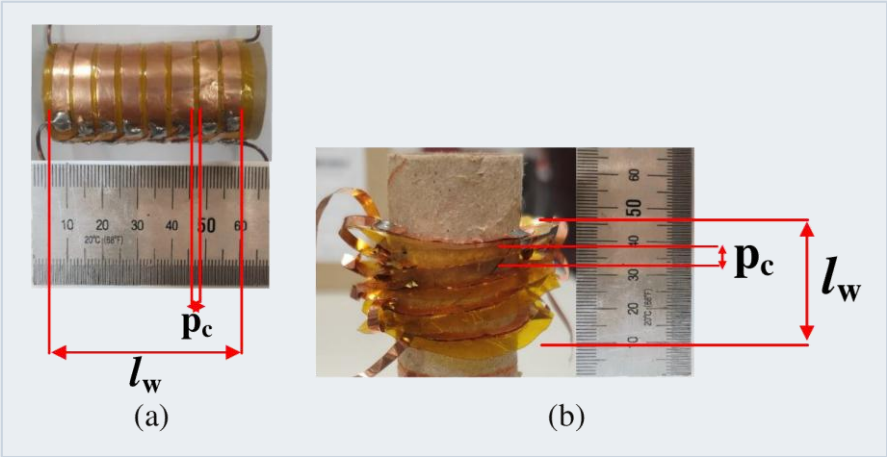


Fig. 27. Copper-foil transformers that raise C_s on purpose: (a) solenoid, (b) comb [6].

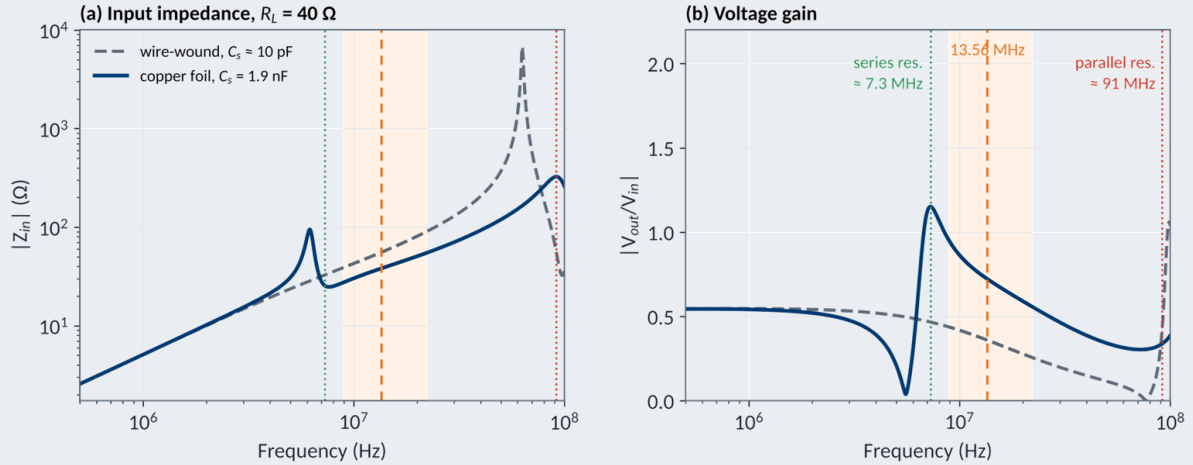


Fig. 28. Model prediction with the measured foil-transformer parameters (L_k = 0.36 µH, L_m = 0.45 µH, C_s = 1.9 nF): the combined path lifts the gain at 13.56 MHz [6].

Gain at 13.56 MHz from the model: ≈0.72 with the foil design versus ≈0.36 for a wire-wound winding with the same inductances

- Air-core MHz transformers have low coupling, so the inductive path alone gives **low gain**
- Wide foil windings raise C_s (≈1.9 nF) and keep C_p low (≈10 pF): series resonance below f_{sw}, parallel resonance well above
- Power then flows through both L_m and C_s [9], [30]

Differential Class-E inverter at 13.56 MHz

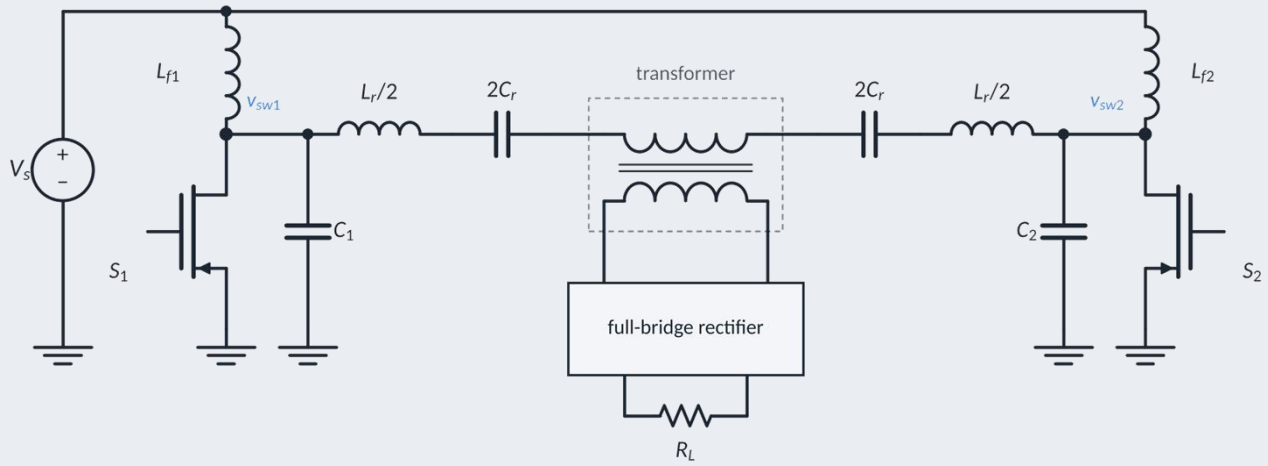


Fig. 29. Differential Class-E inverter with the inductive–capacitive transformer and full-bridge rectifier [6].

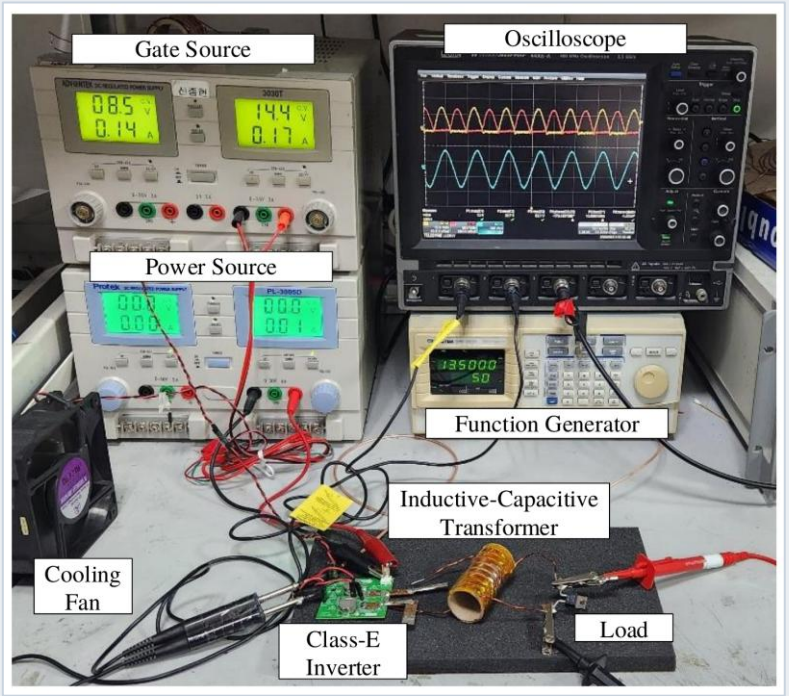


Fig. 30. Experimental set-up with the inductive–capacitive transformer [6].

- Two Class-E legs with complementary gates share one tank; the load sees $v_1 - v_2$
- GaN EPC2207 on EPC9083; rectifier modelled as $R_{ac} = 8R_L/\pi^2$ for the tank design [31]

100 W at 13.56 MHz: more power for the same input

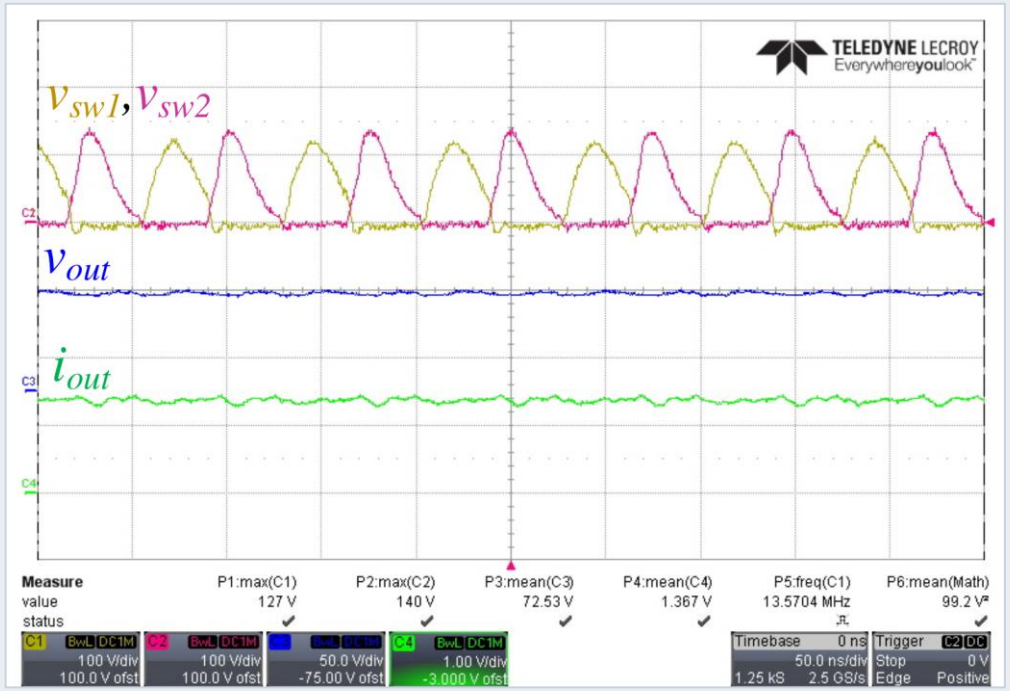


Fig. 31. Foil solenoid transformer at 100 W: v_{sw1}, v_{sw2} (100 V/div), v_{out}, i_{out}; 50 ns/div [6].

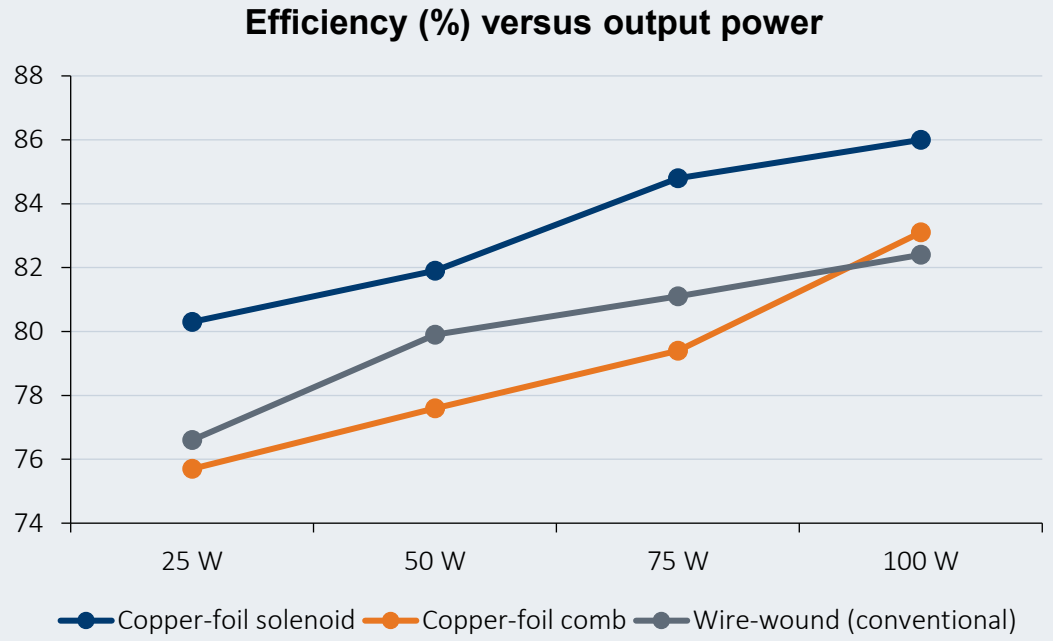


Fig. 32. Measured efficiency, 13.56 MHz, 40 Ω load [6].

86.0 % vs 82.4 %
foil vs wire at 100 W

100 W vs ≈50 W
same ≈33 V input

- ZVS is kept up to 100 W
- Dual inductive–capacitive path raises power density and compensates leakage

Part 6 of 6

Design guidance

Combining this work with the wider literature

Lever 1: winding spacing trades leakage for capacitance

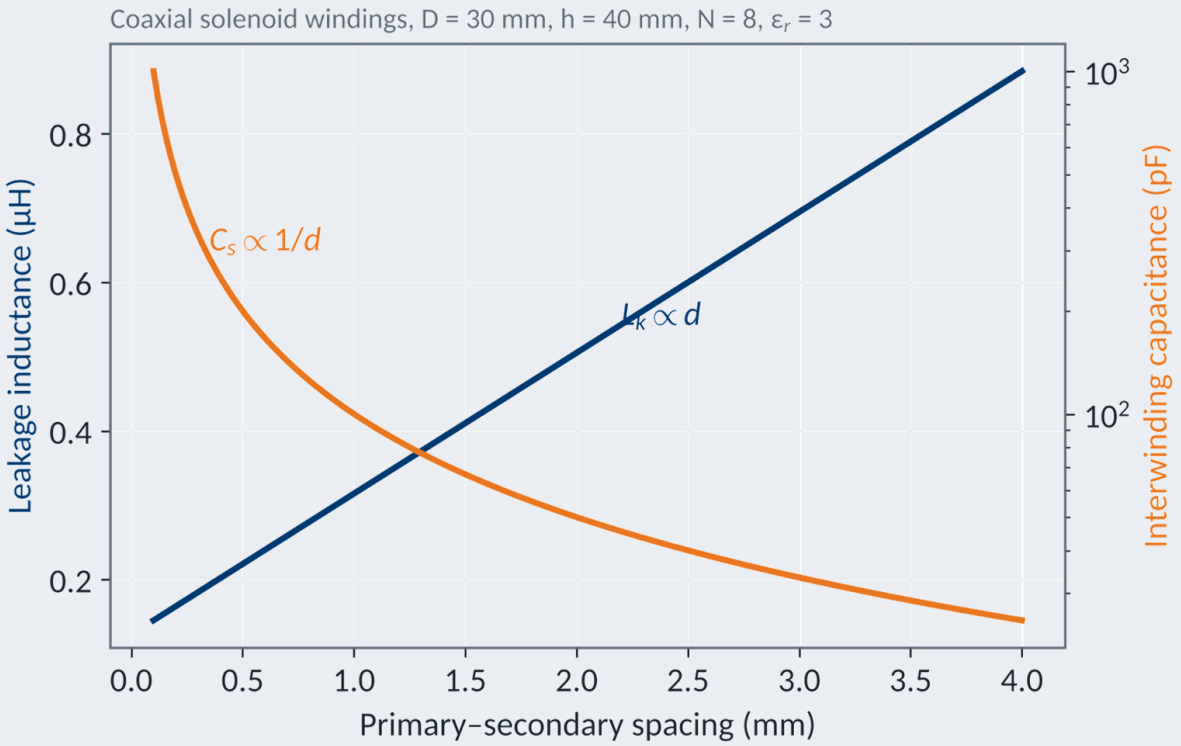


Fig. 33. Approximate leakage and interwinding capacitance of coaxial windings versus spacing (1-D field estimate) [9], [11].

What the physics says

- L_k grows with the gap; C_s falls as 1/gap
- Lower leakage almost always costs capacitance [32]

What the measurements show

- CS4: gap 0.3 → 2 cm gives L_k 3.76 → 6.2 µH and C_s 4 → 2.5 pF [10]
- CS1 → CS3: pitch 10 → 2 mm doubles C_p and gives 7× C_s

Design choice

- Choose the gap for the converter: ZVS margin, CM-noise budget and isolation voltage [5]

Lever 2: winding arrangement

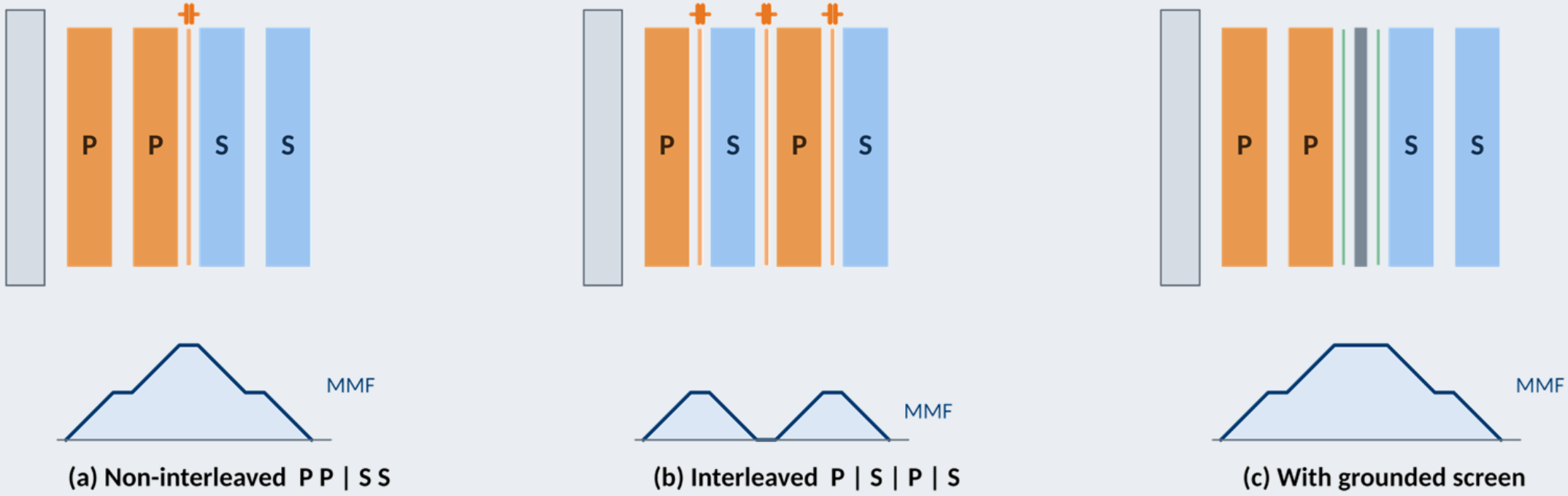


Fig. 34. Layer arrangements: interface capacitances (orange) and MMF distribution [9], [13], [32].

Non-interleaved

One P–S interface: lowest C_s, but high MMF and leakage

Interleaved

Three P–S interfaces: low leakage and AC loss, **highest C_s** and CM noise [32]

Screen / paired layers

Grounded screen or paired layers divert or cancel i_{CM} (≈20 dB) [13]

Lever 3: place the resonances relative to the switching frequency

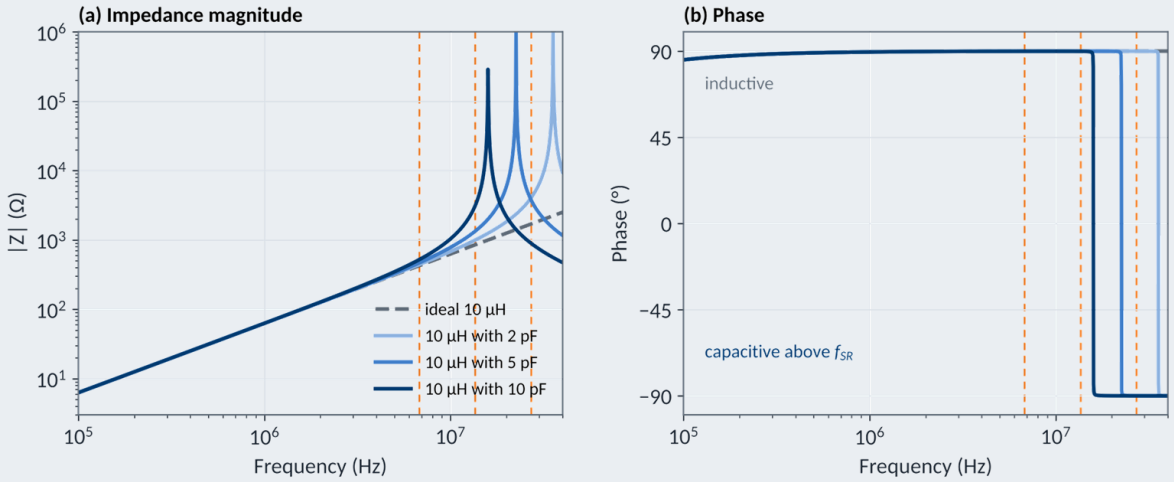


Fig. 35. Self-resonance moves down as C_p grows [11].

For a conventional transformer

- Keep the winding self-resonance **3–5× above f_{sw}**: low pitch-to-wire ratio, few layers, bank or sectioned windings [8], [11]
- Model to at least 2–3× f_{sw} so you can see the first resonance

For an inductive–capacitive transformer

- Put the **series** resonance (C_s with leakage) below f_{sw} for flat gain
- Put the **parallel** resonance (C_p) at least 5× above f_{sw} [6]
- Heavy load: constant-current behaviour; light load: constant-voltage behaviour [6]

Either way

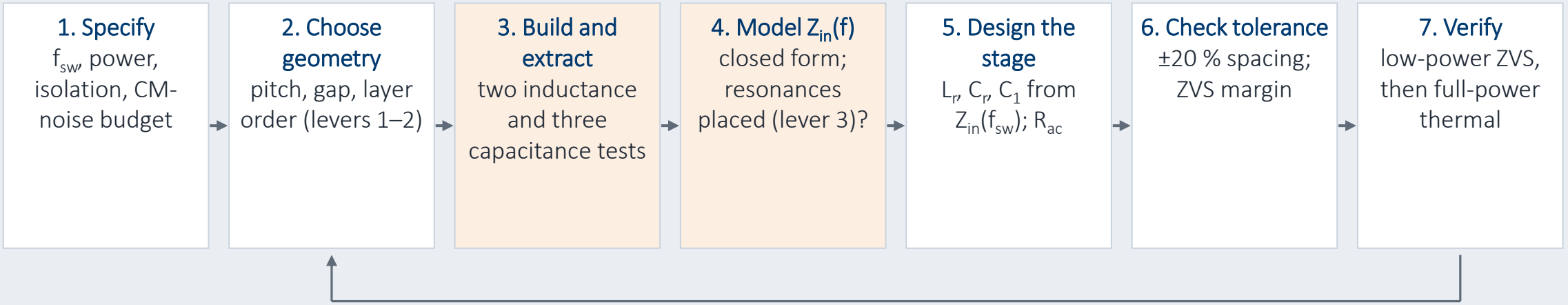
- Absorb every switch-node capacitance (C_{oss}, layout, reflected C_p) into C_1 [12]
- Include transformer C in dead-time and ZVS design [24], [29]

Design rules summarised

Table VI. Practical rules for MHz isolated converters, with supporting work.

#	Rule	Why	Source
1	Measure C_s, C_{p1}, C_{p2} with shorting tests	Analytical values miss the real build	[10], [19]
2	Model Z_{in} with split leakage to ≥ 2–3× f_{sw}	Leakage dominates at MHz	[10]
3	Self-resonance ≥ 3–5× f_{sw}, or design it in	Avoid capacitive loading of the switch	[6], [11]
4	Fold C_{oss}, layout and reflected C into C_1	Class-E ZVS needs the total shunt C	[7], [12]
5	Rectifier as $R_{ac} = 8R_L/\pi^2$	Tank sees the equivalent ac load	[31]
6	Check ±20 % spacing tolerance	Prototype gaps vary	[10]
7	Trade interleaving against CM noise; use screens	C_s sets $i_{CM} = C_s dv/dt$	[13], [32]
8	Place series L with transformer C in mind	Dead-time transition needs it	[24], [29]

A design workflow that reliably reaches soft switching



Measurement tips

- Compensate the fixture (open/short) before each set
- Near resonance |Z| is high and analyser accuracy drops [10]
- Short leads, differential probes; probe C detunes the circuit

Open questions

- Beyond 30 MHz windings become distributed [1]
- Planar/PCB transformers with interleaving at MHz [32]
- Co-design of C for ZVS, EMI and isolation together [5]

Key takeaways

1	The ideal transformer fails at MHz	Picofarad intra- and interwinding capacitances resonate with leakage and magnetising inductance in the 3–30 MHz range.
2	Picofarads decide soft switching	$Z_{in}(f_{sw})$ sets the tank and C_1; a few-percent error loses ZVS and adds ½CV^2f loss and CM noise.
3	A simple physical model is enough	Split leakage plus three lumped capacitors, from five measurements, gives a closed-form Z_{in}.
4	Validated to 30 MHz and in hardware	At 13.56 MHz: efficiency 31 → 68 %, switch 75 → 42 °C; foil ICPT transformer 86 % at 100 W.
5	Design with the parasitics	Choose spacing and layer order for ZVS, EMI and isolation, or use C_s as a power path.

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